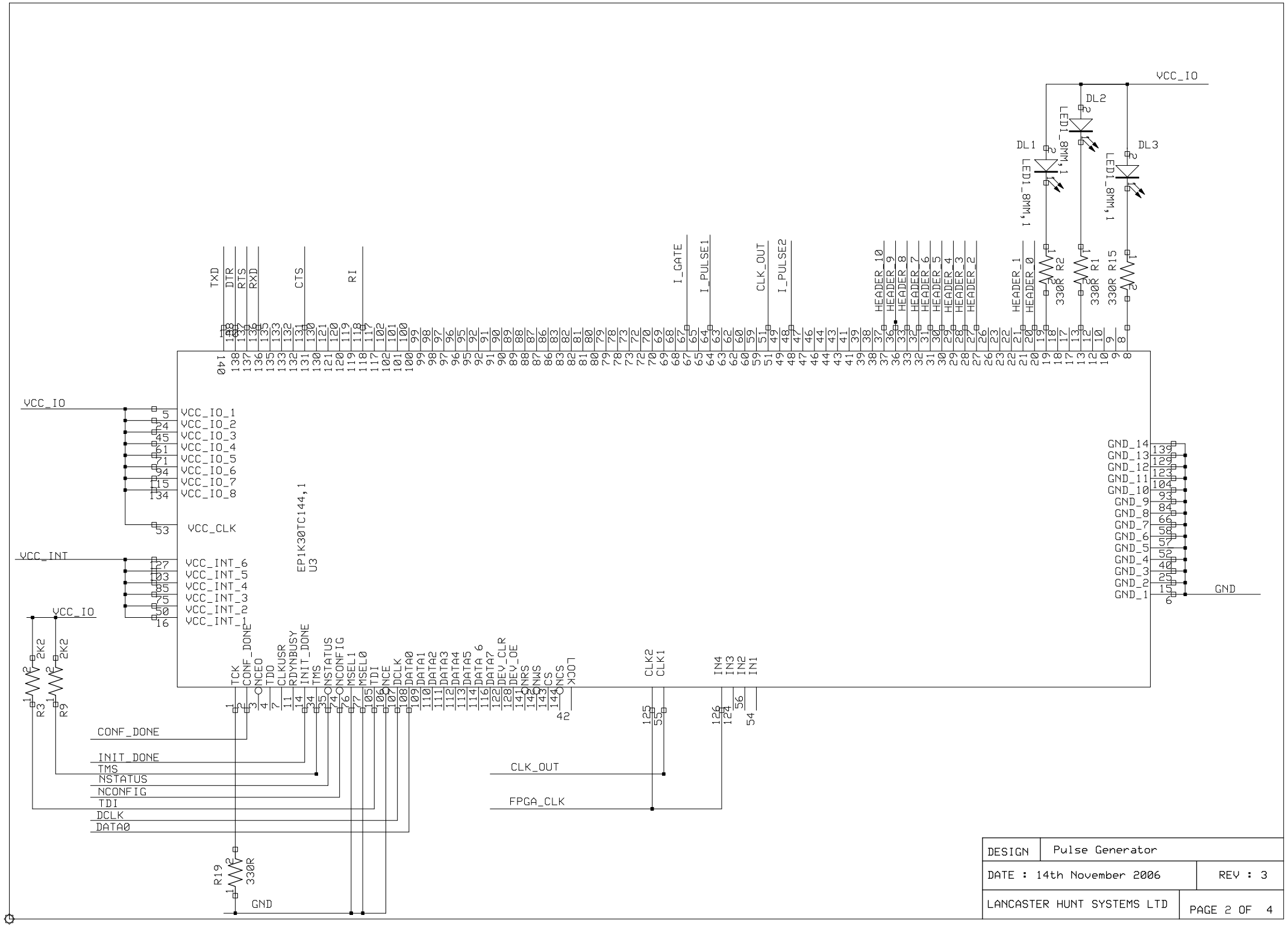
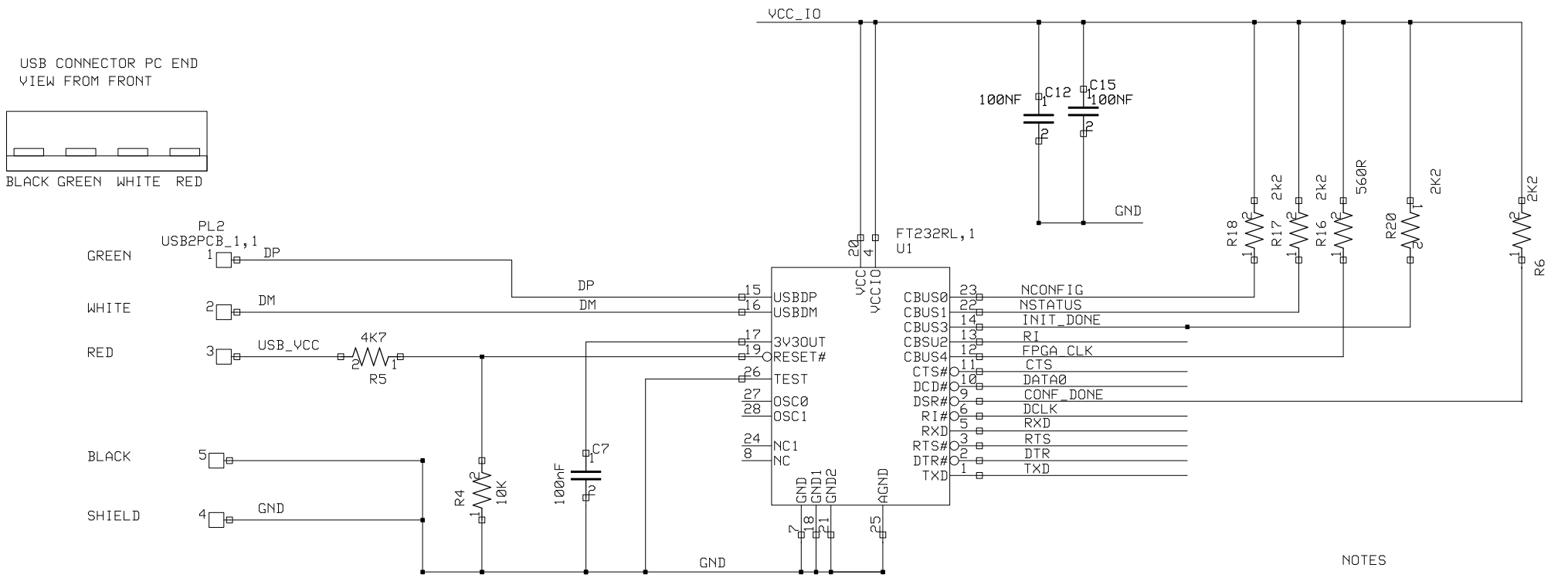


DESIGN	Pulse Generator
DATE : 14th November 2006	REV : 3
LANCASTER HUNT SYSTEMS LTD	PAGE 2 OF 4

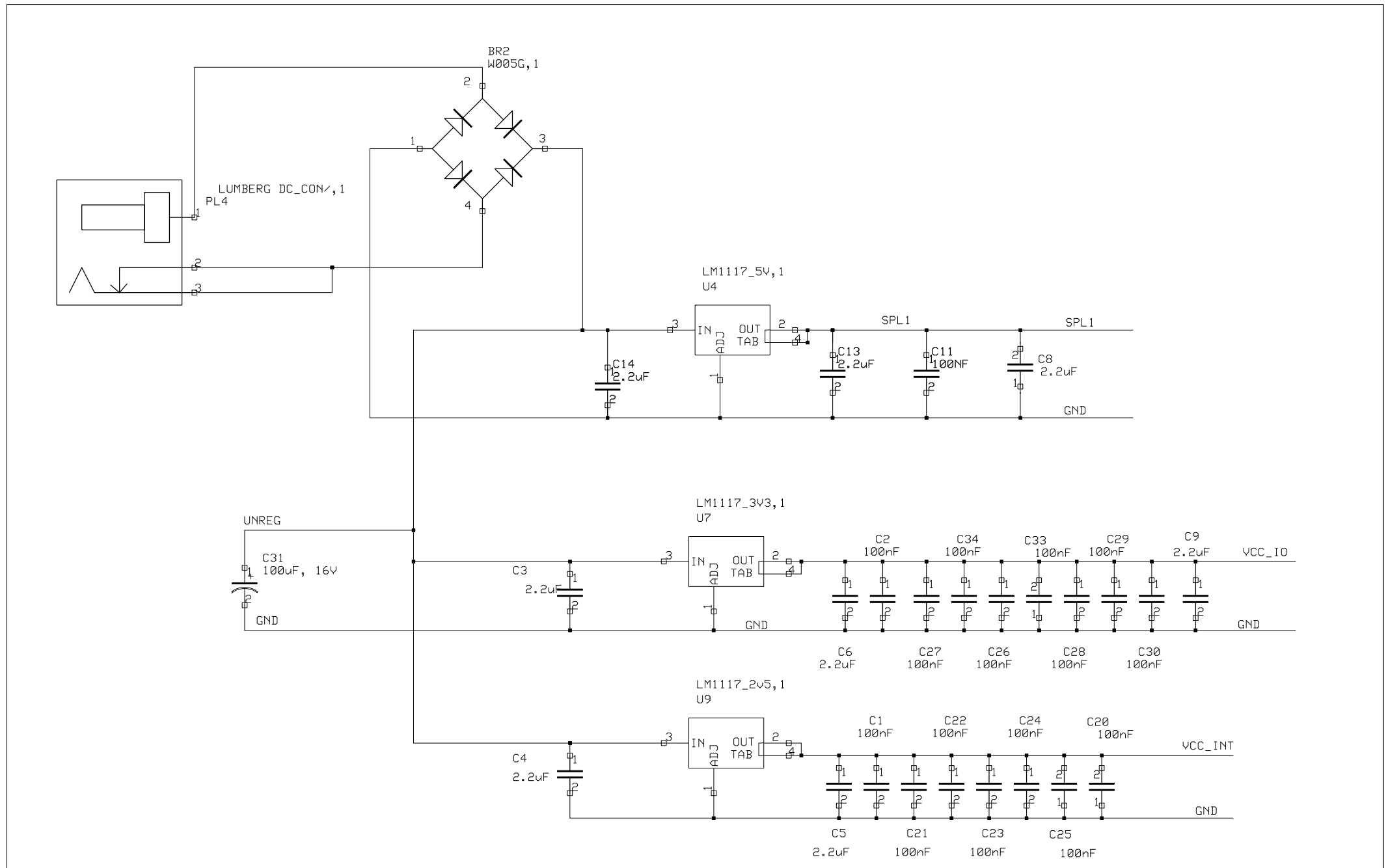


NOTES

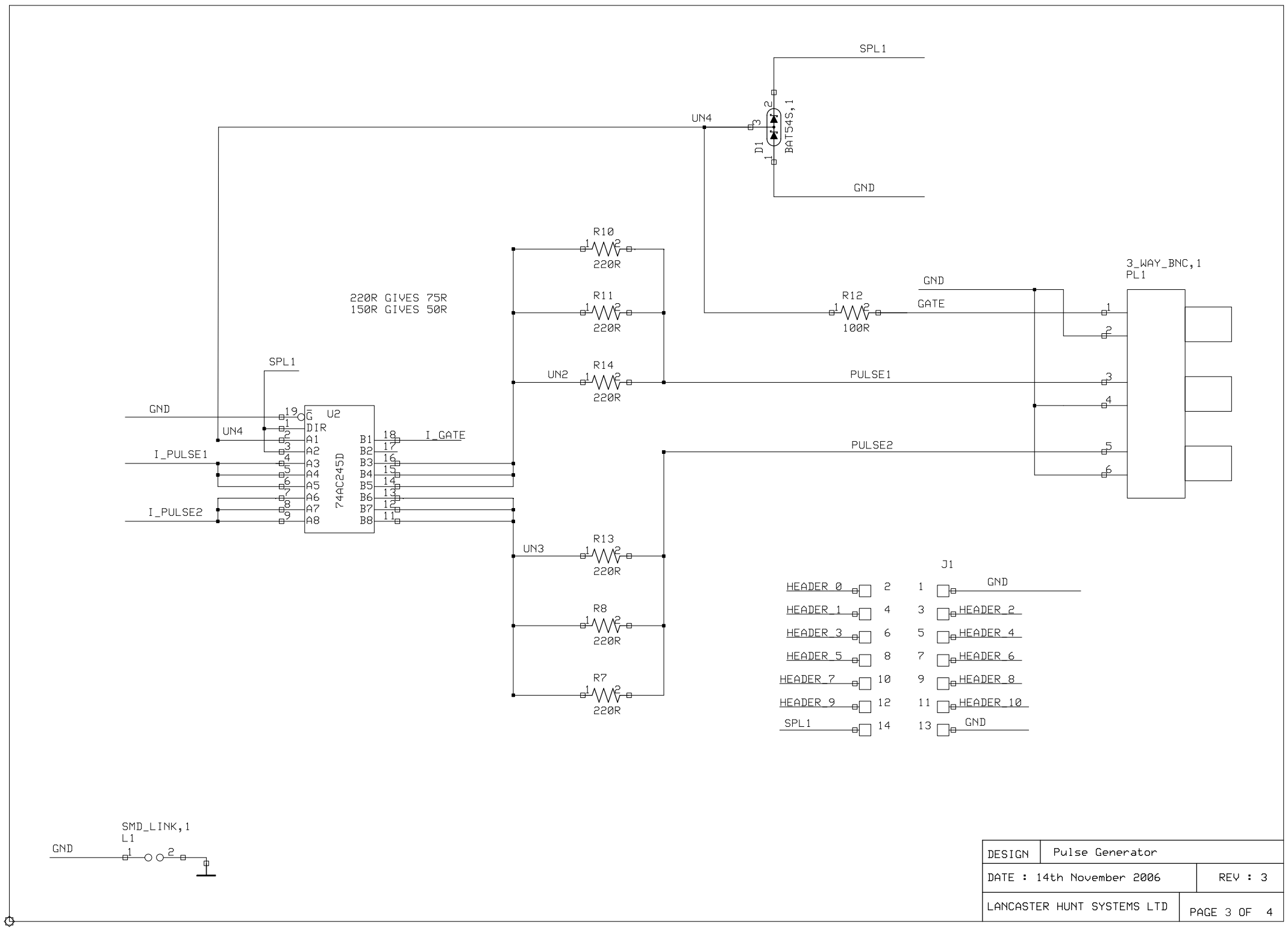
USE RTS/CTS FLOW CONTROL

USE DTR AS A RESET FOR THE FPGA

DESIGN	Pulse Generator
DATE : 14th November 2006	REV : 3
LANCASTER HUNT SYSTEMS LTD	PAGE 4 OF 4



DESIGN	Pulse Generator
DATE : 14th November 2006	REV : 3
LANCASTER HUNT SYSTEMS LTD	PAGE 1 OF 4



DESIGN	Pulse Generator
DATE : 14th November 2006	REV : 3
LANCASTER HUNT SYSTEMS LTD	PAGE 3 OF 4