

A Briefing on IEEE 1149.1 –1990 Standard Test Access Port And Boundary-Scan Architecture (AKA JTAG)

Summary

With the advent of large Ball Grid Array (BGA) and fine pitch SMD semiconductor devices the ability to test and debug PCBs using traditional methods has been greatly reduced. New techniques are required to allow acceptable levels of board level test to be obtained. IEEE1149.1 (AKA JTAG or Boundary Scan) is the predominant of these technologies. This document outlines the reasons for using JTAG and the advantages gained through its use.

JTAG = Joint Action Test Group – this was the result of thousands of man-hours of co-operative development by approximately 200 major international electronics firms.

Scope

This document provides information on the IEEE 1149.1–1990 standard. It assumes a familiarity with current test methods and techniques.

This document is not intended to be an in-depth primer on the standard as many excellent examples already exist. (See Resources) This documents does provide a brief introduction to the standard, the motivation behind its inception, the current uses and the pros and cons of implementation.

A large part of this document is devoted to providing pointers for further reading and enlightenment.

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1. The Problem

Since the mid-1970s, the testing of loaded PCBs has relied on the use of the in-circuit "bed of nails" technique. This method of testing makes use of a fixture containing a "bed of nails" to access individual devices on the board through test pads or other convenient contact points, such as IC pins and connectors.

With increasing use of new PCB and semiconductor packaging technologies it is difficult, sometimes impossible, to probe a PCB using "bed of nails" methods. For example, consider that it is possible to build a PCB with only BGA components, using blind vias and buried capacitance and resistive layers in the PCB. This PCB need have no external probing points.

The problem can be defined as follows:

1.1. Increased Use Of SMD

- 1.1.1. The use of SMD components reduces the number of signals that can be probed using bed of nails techniques.

1.2. Fine Pitch components

- 1.2.1. With lead pitches getting down to 0.5mm, it is difficult to probe ICs in all situations.
- 1.2.2. Probing can cause electrical damage to the PCB due to shorting of pins.
- 1.2.3. Providing test points on these devices can cause PCB layout issues due to limited routing resources.

1.3. BGA and Chip Scale Packaging

- 1.3.1. Increasing use of BGA and chip scale packaging techniques in semiconductor devices means that IC pins are no longer available for probing.
- 1.3.2. Providing test points on these devices can cause PCB layout issues due to limited routing resources.

1.4. Conformal Coating.

- 1.4.1. Conformal coatings can prevent access to device leads and test points.

1.5. Small PCB geometry's.

- 1.5.1. With PCBs getting smaller and more complex. It can be difficult to get access to all the required test points.

- 1.5.2. Provisioning all signals with at least two test points uses a significant amount of board real estate.

1.6. Comes down to these issues –

- 1.6.1. Increasing circuit complexity.
- 1.6.2. Decreasing board areas.
- 1.6.3. Limited component access.

2. A Solution - Boundary Scan.

Back in the 80s a group of manufacturers realised that this problem was brewing. A group of, eventually 200, companies formed an interest group to investigate the problems highlighted. The outcome of all this was a test methodology called boundary scan. This was accepted as an IEEE standard in 1990. It is formally known as IEEE1149.1 1990, commonly known as JTAG or Boundary Scan. There has been one major revision in 1993.

The test philosophy is based on statistics that show that the majority of board defects are found in the periphery of devices. Faults are commonly found as:

- PCB Interconnection faults. Commonly shorts and opens in the PCB.
- IC interconnection faults. Commonly wire bonding issues, or damage to input buffers or output drivers.

It is very uncommon for a device to fail due to damage to the core circuitry.

2.1. Boundary Scan Is designed to address needs in:

2.1.1. Prototype development

Is the fault due to manufacturing defects or due to design issues?

Completing a boundary scan of the PCB will quickly reveal manufacturing issues, allowing the designer to concentrate on finding the design issues.

Boundary Scan can also interrogate internal registers, provide ICE facilities and access BIST functions inside devices.

2.1.2. Integration and test

JTAG can be used to provide access to internal registers and pin conditions. This can be used for example when a CPU is stuck.

2.1.3. Manufacturing test

Fast JTAG testers are used to detect manufacturing defects in the production process.

2.1.4. Field service test

Many JTAG testers consist of a PC with an adapter cable. So it is possible to test field failures in situ.

2.1.5. Remote test

A JTAG tester can be built into the PCB or as part of the system design. This allows for remote failure diagnosis.

2.1.6. Built In Self Test (BIST)

JTAG can access internal device registers, which can control BIST operations. This can be achieved at the board level or at the system level.

Some high reliability systems do self -tests using JTAG to prove system robustness before becoming operational. This allows for a high degree of system fault diagnosis.

2.2. Boundary Scan Provides the following test functions :

2.2.1. Test the operation of the device core.

2.2.2. Test PCBs for short/open circuits.

2.2.3. Test the function of non-JTAG chips using the JTAG port of the neighbouring devices.

2.3. Boundary scan works as follows :

2.3.1. Each device has a set of registers. These registers give access to :

- Monitor points situated on all inputs.
- Drive points on all outputs.

2.3.2. Using the monitor and drive points between different devices it is possible to check for opens, shorts and run functional tests.

2.4. Each device has a 4 wire Test Access Port (TAP).

2.4.1. TAP provides access to test functions built into the component.

2.4.2. Requires a minimum 4 signals

- TMS - Test Modes Select
- TDI – Test Data In
- TDO – Test Data Out
- TCK – Test Clock

2.5. Several devices can be daisy-chained onto the same JTAG connection. This concept can be expanded to include multiple boards, sub systems or complete installation.

2.6. The data transfer is controlled by a state machine, which is driven by TMS and TCK. Through this data and instructions are passed to/from the test controller.

2.7. Device contains registers that are accessed through the TAP. The minimum set of registers is :

2.7.1. Bypass – 1 bit cell which connects TDI to TDO

2.7.2. Boundary Scan – n bit shift register which connects TDI to TDO. Each IO pin of the device gets 1 bit of the register.

2.7.3. Device ID – identification of the device

2.8. Minimum test requirements are :

2.8.1. All inputs must be viewable.

2.8.2. All outputs must be controllable.

2.9. *Manufacturers. Can include proprietary test functions and access them through the TAP.*

2.9.1. This allows for BIST functionality to be integrated with boundary scan testing.

2.10. *Recent addition is programming of FPGAs/CPLDs and embedded microprocessors.*

2.10.1. Most modern FPGAs and CPLDs are able to be programmed using JTAG ports.

2.10.2. Some of the highly integrated microprocessors are also programmable via JTAG.

2.10.3. In case of Flash based devices this allows for un-programmed parts to be placed. Which has advantages in inventory control.

2.10.4. In all cases this allows for functional test programs to be downloaded. Then overwritten by the operational software.

2.11. *JTAG can allow real time access to internal device registers. This can be used for ICE type functionality in microprocessors*

2.11.1. Some CPU manufacturers have taken advantage of the JTAG port, to give access to internal registers whilst the CPU is running. This allows for low cost In Circuit Emulation and debugging techniques to be applied.

3. Advantages

3.1. Enables testing for correct device placement.

Using the Device ID it is possible to check the correct device is in the correct position.

3.2. Enables detection of device failures.

JTAG can be used to access BIST modules within a design.

3.3. Enables the detection of shorts and opens.

Shorts and opens can be detected by using JTAG to drive signals on to circuits and monitor the response. It is possible to generate sophisticated diagnostic programs that can identify where the problems are.

3.4. Enables full functional testing.

It is equally possible to run a full board level functional test using JTAG.

3.5. Can be used for device programming.

Many FPGAs, CPLDs and embedded processors use a JTAG port to support in circuit programming. This enables manufacturers to keep stock of un-programmed devices and only program them when used.

3.6. Testing is fully automated

JTAG testing can be completely automated. The test software can be written to give detailed diagnostic information, such as short between U115 pin4 and U12 pin 9.

3.7. Design functions can use JTAG to verify board quality during debugging.

Designers find JTAG is very useful in debugging prototype circuits. The ability to test that a PCB has not developed manufacturing faults can save a lot of time.

4. Disadvantages

4.1. Can be difficult to get 100% test coverage.

Not all devices support JTAG and to get good test coverage and maximise diagnostic information, it is best to have at least two JTAG pins per net.

4.2. JTAG is a large overhead in smaller devices.

Because JTAG requires 4 pins as a minimum, it is a large overhead in devices under 50 pins. Because of this JTAG is predominantly used on devices over 100 pins.

4.3. Not much use for analog devices.

JTAG is a digital test scheme. If the board is mainly analog, other test methods are better. There is a JTAG standard for mixed signal devices, but this is relatively new.

4.4. PCB Layout Issues.

The scan chain has to be laid out to provide good signal integrity. Incorrect operation and false entry into JTAG modes can occur if the signals are not treated as critical nets. If several devices are in the chain, then the TCK and TMS signals must be de-skewed to preserve correct operation.

4.5. Provision of test programs.

Each device has a unique JTAG model, which has to be incorporated into a test program. A full production test program is a major undertaking. Ideally the program should be written and tested before the prototype design stage.

4.6. Provision of library models.

Some manufacturers have been known to be tardy over the release of the BSDL models. Some models have been proven to be inaccurate.

5. Resources

5.1. General Information

- 5.1.1. Design for test Presentation.
<http://www.erc.msstate.edu/~reese/EE4743/designfortest/tsld001.htm>
- 5.1.2. IEEE 1149.1 Application Notes from TI
http://www.ti.com/sc/docs/apps/logic/boundary_scan_jtag_logicapp.html
- 5.1.3. BSDL/IEEE 1149.1 Verification Service from Aligent
http://www.agilent.com/see/bsdl_service.
- 5.1.4. On-line tutorial form Asset
<http://www.asset-intertech.com/tutorial/tutorial.htm>
- 5.1.5. IEEE - Place to buy your specification.
<http://www.ieee.org/>
- 5.1.6. Xilinx Guide to JTAG
http://toolbox.xilinx.com/docsan/3_1i/data/common/jtg/dppa/appa.htm
- 5.1.7. Sun White paper on JTAG
<http://www.sun.com/microelectronics/whitepapers/wpr-0018-01>
- 5.1.8. National Semiconductor JTAG site.
<http://www.national.com/appinfo/scan/index.html>

5.2. Books

- 5.2.1. K. Parker, "The Boundary-Scan Handbook, Analog and Digital"
Kluwer Academic Publishers, 1998 Second Edition
(Very good chapters on BSDL and on DFT guidelines)
- 5.2.2. H. Bleeker et al., "Boundary-Scan Test: A Practical Approach,"
Kluwer Academic Publishers, 1993
(The "Philips" approach, including a chapter targeted on managers)
- 5.2.3. Latest issues of IEEE ITC Proceedings; Journal of Electrical Test: Theory and
Application (Kluwer Academic Press);
IEEE Design & Test of Computers

- 5.2.4. 1149.1 IEEE Standard Test Access Port and Boundary-Scan Architecture.
IEEE, Piscataway, NJ

5.3. Test Equipment

- 5.3.1. Asset Technology - Boundary scan testing and programming.
<http://www.asset-intertech.com/boundaryscan.htm>
- 5.3.2. Goepel - Boundary scan testing and programming.
<http://www.goepel.com/english/news/newsbsc.htm>
- 5.3.3. Manufacturers of test and programming equipment.
<http://www.diagnosys.com>
- 5.3.4. JTAG Technologies BV. Incircuit test and programming.
<http://www.jtag.com>
- 5.3.5. Corelis Jtag board testers and In Circuit Emulators.
<http://www.jtag.org>
- 5.3.6. A.T.E. (Advanced Test Engineering) Solutions, Inc. Test related products and services.
<http://www.besttest.com>
- 5.3.7. Genrad In Circuit Test Equipment. With JTAG support
<http://www.genrad.com/ems/incircuit/teststation.html>
- 5.3.8. Wayne Kerr – general circuit test equipment with JTAG support.
<http://www.wkelectronics.com>
- 5.3.9. Logicvision - board level JTAG test equipment.
http://www.logicvision.com/solution/jtag_xli.htm

5.4. Training

- 5.4.1. Aligent training courses.
http://contact.tm.agilent.com/tmo/education/English/E3795C_US.html
- 5.4.2. Home of scan educator, a free training course.
<http://www.ti.com/sc/docs/jtag/educ.htm>

5.5. Articles

- 5.5.1. Boundary-Scan Software Aids PCB Evaluation
Test & Measurement World, October 1999
http://www.tmworld.com/articles/10_1999_PCB.htm

- 5.5.2. Design Techniques Ensure Testable SOCs
Test & Measurement World, September 1999
http://www.tmworld.com/articles/09_1999_Design_SOCS.htm
- 5.5.3. Design a Production and Test Strategy for PLD-Based PCBs, Part 2
Test & Measurement World, March 1999
http://www.tmworld.com/articles/03_1999_onboard_part2.htm
- 5.5.4. Boundary Scan Design for Board Testability and In-Circuit programming
Industry Access
<http://www.industryaccess.com.au/articles/10018.shtml>
- 5.5.5. Designing With Boundary Scan
Insideelectronics
<http://www.insideelectronics.com/test/archive/dft/bae1198.html>
- 5.5.6. DFT Techniques For Boundary Scan
Insideelectronics
<http://www.insideelectronics.com/test/archive/dft/dft1098.html>
- 5.5.7. The Chain Of Confidence
Insideelectronics
<http://www.insideelectronics.com/test/archive/dft/bs1298.html>

5.6. Software

- 5.6.1. Synopsis BSDL compiler
http://www.synopsys.com/news/announce/press/bsdtest_pr.html
- 5.6.2. Syntest TurboBSD BSDL compiler
<http://www.syntest.com>
- 5.6.3. Teradyne software integrates boundary scan with other test methods
<http://www.teradyne.com/prods/cbt/products/pVICT/pVICT.html>
- 5.6.4. Asset Intertech BSDL compilers etc.
<http://www.asset-intertech.com>
- 5.6.5. Intellitech provide BSDL compilers and JTAG support software.
<http://www.intellitech.com>

5.7. In Circuit Programming

- 5.7.1. Altera
<http://www.altera.com/html/mktg/isp.html>
- 5.7.2. Lattice
<http://www.latticesemi.com>

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5.7.3. Xilinx

<http://www.xilinx.com>

5.7.4. Actel

<http://www.actel.com>

5.7.5. Cypress

<http://www.cypress.com>

5.8. ASIC Synthesis

5.8.1. Mentor JTAG synthesis tools.

http://www.mentor.com/bsdarchitect/bsdarchitect_ds.html

5.8.2. Veritools - JTAG Test Synthesis for ASIC and IC Designers

<http://www.veritools-web.com/vbit.htm>

5.8.3. Opencores Organisation offer a freeware JTAG implementation.

<http://www.opencores.org>